PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shahrokh Shahidzadeh	)	Examiner: Tang, Son M.
Serial No.: 10/676,178	)	Art Unit: 2612
Filed: 09/30/2003	)	
For: **Event Signature Apparatus Systems, and Methods**	)	
Date of Last Office Action:	)	Attorney Docket No.: 28336-00003

CERTIFICATE OF MAILING UNDER 37 C.F.R. 1.8

Dear Sir:

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Date: October 31, 2007

Items enclosed herewith:

1. Appeal Brief
2. Transmittal
3. Check in the amount of $510
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PTO/SB/17 (12-04v2)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	510.00

Complete if Known	
Application Number	10/676,178
Filing Date	09/30/2003
First Named Inventor	Shahrokh Shahidzadeh
Examiner Name	Son M. Tang
Art Unit	2612
Attorney Docket No.	28336-00003

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: _____ Deposit Account Name: _____

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Multiple Dependent Claims Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round **up** to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Fee for Appeal Brief	510.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 38,520	Telephone (216) 348-5844
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shahrokh Shahidzadeh	Examiner: Tang, Son M
	Art Unit: 2612
Serial No.: 10/676,178	
Filed: September 30, 2003	
For: EVENT SIGNATURE APPARATUS, SYSTEMS, AND METHODS	
Date of Final Office Action: February 23, 2007	Attorney Docket No.: 28336-00003
Notice of Appeal Filed: October 10, 2007	

October 31, 2007

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is timely provided to support the Notice of Appeal filed October 10, 2007.

1. Real Party in Interest:

The real party in interest is Intel Corporation, a Delaware corporation headquartered at 2200 Mission College Boulevard, Santa Clara, California, 95054.

2. Related Appeals and Interferences

There are no other prior and/or pending appeals, interferences, or judicial proceedings that are related to, directly affect, or that will be directly affected by or have a bearing on the Board's decision.

3. Status of Claims

Claims 1-29 are pending for examination.

Claims 1-29 stand rejected in the application.

The rejections of claims 1-29 are appealed.

4. Status of Amendments

No Amendments were filed subsequent to the Final Office Action.

5. Summary of Claimed Subject Matter

Independent Claim 1

Claim 1 recites a method that comprises storing data corresponding to at least one input operating over-voltage condition occurring in an integrated circuit in an indelible memory. One structure that corresponds to the claimed function is MEM 114. (Specification, Page 3, Lines 8-10; Figure 1, MEM 114; Specification, Page 7, Lines 23-25; Page 8, Lines 11-12; Figure 4, Block 461).

Independent Claim 4

Claim 4 is directed to a method comprising comparing an input operational condition with a specified condition. One structure that corresponds to the claimed function is COMPARE 126. (Specification, Page 7, Lines 18-19; Figure 1, COMPARE 126; Figure 4, Block 441; Figure 5, Block 591). Claim 4 recites recording data corresponding to an out-of-specification input operating condition in an indelible memory. One structure that corresponds to the claimed function is MEM 114. (Specification, Page 7, Lines 23-25; Figure 1, MEM 114; Figure 4, Block 461; Figure 5, Block 595). The method of claim 4 further comprises determining a specified number of recorded out-of-specification input operating conditions. One structure that corresponds to the claimed function is BIOS 154. (Specification, Page 5, Lines 5-10; Figure 1, BIOS 154; Page 7, Lines 28-29; Figure 4, Blocks 471 and 481; Figure 5, Block 595).

Dependent claim 7

Claim 7 recites a method comprising comparing an input operational condition with a specified condition. One structure that corresponds to the claimed function is COMPARE 126. (Specification, Page 7, Lines 18-19; Figure 1, COMPARE 126; Figure 4, Block 441; Figure 5, Block 591). Claim 7 further recites recording data corresponding to an out-of-

specification input operating condition in an indelible memory. One structure that corresponds to the claimed function is MEM 114. (Specification, Page 7, Lines 23-25; Figure 1, MEM 114; Figure 4, Block 461; Figure 5, Block 595). Claim 4 also recites determining a specified number of recorded out-of-specification input operating conditions. One structure that corresponds to the claimed function is BIOS 154. (Specification, Page 5, Lines 5-10; Figure 1, BIOS 154; Page 7, Lines 28-29; Figure 4, Blocks 471 and 481; Figure 5, Block 595). Further, claim 4 recites refraining from detecting the out-of-specification input operating condition for a specified amount of time (Specification, Page 7, Lines 11-13; Figure 4, Block 425), wherein the specified amount of time is associated with a power-on reset time. (Specification, Page 7, Lines 13-15).

Dependent claim 9

Claim 9 claims a method comprising comparing an input operational condition with a specified condition. One structure that corresponds to the claimed function is COMPARE 126. (Specification, Page 7, Lines 18-19; Figure 1, COMPARE 126; Figure 4, Block 441; Figure 5, Block 591). Claim 9 further claims recording data corresponding to an out-of-specification input operating condition in an indelible memory. One structure that corresponds to the claimed function is MEM 114. (Specification, Page 7, Lines 23-25; Figure 1, MEM 114; Figure 4, Block 461; Figure 5, Block 595). Further claim 9 claims determining a specified number of recorded out-of-specification input operating conditions. One structure that corresponds to the claimed function is BIOS 154. (Specification, Page 5, Lines 5-10; Figure 1, BIOS 154; Page 7, Lines 28-29; Figure 4, Blocks 471 and 481; Figure 5, Block 595), wherein recording the out-of-specification input operating condition further comprises recording a clock speed. (Specification, Page 2, Line 27 – Page 3, Line 2).

Dependent claim 11

Claim 11 is directed to a method comprising comparing an input operational condition with a specified condition. One structure that corresponds to the claimed function

is COMPARE 126. (Specification, Page 7, Lines 18-19; Figure 1, COMPARE 126; Figure 4, Block 441; Figure 5, Block 591). The method of claim 11 also comprises recording data corresponding to an out-of-specification input operating condition in an indelible memory. One structure that corresponds to the claimed function is MEM 114. (Specification, Page 7, Lines 23-25; Figure 1, MEM 114; Figure 4, Block 461; Figure 5, Block 595). Further, the method of claim 11 comprises determining a specified number of recorded out-of-specification input operating conditions. One structure that corresponds to the claimed function is BIOS 154. (Specification, Page 5, Lines 5-10; Figure 1, BIOS 154; Page 7, Lines 28-29; Figure 4, Blocks 471 and 481; Figure 5, Block 595), wherein determining the specified number of recorded out-of-specification input operating conditions further comprises reading a signature value stored in the indelible memory. (Specification, Page 5, Lines 25-30; Page 8, Lines 3-6; Figure 4, Block 475).

Independent Claim 12

Claim 12 recites an article comprising a machine-accessible medium having associated data (Specification, Page 9, Lines 19-26; Figure 5, Blocks 589 and 591), wherein the data, when accessed, results in a machine comparing an input operational voltage with a specified voltage, recording a value corresponding to an input operating over-voltage condition in an indelible memory, and determining a specified number of recorded input operating over-voltage conditions. (Specification, Page 9, Lines 26-29; Figure 4, Blocks 441, 461, and 471).

Dependent claim 13

Claim 13 claims an article comprising a machine-accessible medium having associated data (Specification, Page 9, Lines 19-26; Figure 5, Blocks 589 and 591), wherein the data, when accessed, results in a machine comparing an input operational voltage with a specified voltage, recording a value corresponding to an input operating over-voltage condition in an indelible memory, and determining a specified number of recorded input

operating over-voltage conditions (Specification, Page 9, Lines 26-29; Figure 4, Blocks 441, 461, and 471), wherein the data, when accessed, results in the machine filtering the input operational voltage for at least a duration of one clock period. (Specification, Page 9, Line 29 – Page 10, Line 1).

Dependent claim 14

Claim 14 is directed to an article comprising a machine-accessible medium having associated data (Specification, Page 9, Lines 19-26; Figure 5, Blocks 589 and 591), wherein the data, when accessed, results in a machine comparing an input operational voltage with a specified voltage, recording a value corresponding to an input operating over-voltage condition in an indelible memory, and determining a specified number of recorded input operating over-voltage conditions (Specification, Page 9, Lines 26-29; Figure 4, Blocks 441, 461, and 471), wherein recording the value corresponding to the input operating over-voltage condition further comprises recording the value corresponding to the input operating over-voltage condition only if the input operational voltage is greater than the specified voltage by a selected amount. (Specification, Page 9, Line 29 – Page 10, Line 3).

Dependent claim 15

Claim 15 claims an article comprising a machine-accessible medium having associated data (Specification, Page 9, Lines 19-26; Figure 5, Blocks 589 and 591), wherein the data, when accessed, results in a machine comparing an input operational voltage with a specified voltage, recording a value corresponding to an input operating over-voltage condition in an indelible memory, and determining a specified number of recorded input operating over-voltage conditions (Specification, Page 9, Lines 26-29; Figure 4, Blocks 441, 461, and 471), wherein recording the value corresponding to the input operating over-voltage condition further comprises recording the value corresponding to the input operating over-voltage condition only if the input operational voltage is greater than the specified voltage by

a selected amount at least about two times greater than an expected noise voltage value. (Specification, Page 9, Line 29 – Page 10, Line 4).

Dependent claim 16

Claim 16 recites an article comprising a machine-accessible medium having associated data (Specification, Page 9, Lines 19-26; Figure 5, Blocks 589 and 591), wherein the data, when accessed, results in a machine comparing an input operational voltage with a specified voltage, recording a value corresponding to an input operating over-voltage condition in an indelible memory, and determining a specified number of recorded input operating over-voltage conditions (Specification, Page 9, Lines 26-29; Figure 4, Blocks 441, 461, and 471). Claim 16 further recites that when the data is accessed the machine verifies recordation of the value corresponding to the input operating over-voltage condition. (Specification, Page 9, Line 29 – Page 10, Line 4; Figure 4, Block 465).

Independent Claim 17

Claim 17 is directed to an apparatus comprising an indelible memory to store information corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit. (Specification, Page 3, Lines 7-11; Figure 1, Apparatus 100).

Dependent claim 19

Claim 19 recites an apparatus comprising an indelible memory to store information corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit (Specification, Page 3, Lines 7-11; Figure 1, Apparatus 100), a detection module coupled to the indelible memory to determine the existence of at least one of the selected number of out-of-specification input operational conditions

(Specification, Page 3, Lines 12-14; Figure 1, DETECT 122), and a filter module coupled to the detection module (Specification, Page 4, Lines 14-15; Figure 1, F 138).

Independent Claim 22

Claim 22 recites a system comprising an indelible memory to store data corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit. (Specification, Page 4, Lines 23-25; Figure 1, System 110). The system of claim 22 further comprises a display coupled to the electronic circuit. (Specification, Page 4, Lines 23-25; Figure 1, DISPLAY 140).

Dependent claim 29

Claim 29 is directed to a system comprising an indelible memory to store data corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit (Specification, Page 4, Lines 23-25; Figure 1, System 110). The system of claim 29 further comprises a display coupled to the electronic circuit (Specification, Page 4, Lines 23-25; Figure 1, DISPLAY 140), and a basic input-output system to determine the selected number of out-of-specification input operational conditions. (Specification, Page 5, Lines 3-10; Figure 1, BIOS 154).

6. Grounds of Rejection to be Reviewed on Appeal

The following grounds of rejection are to be reviewed on appeal:

I. Whether claims 1-29 are unpatentable under 35 U.S.C. §103(a) over Chevallier (U.S. Patent No. 5,898,634) in view of Mori et al. (U.S. Patent No. 6,891,214), and further in view of Perner (U.S. Patent No. 6,694,282).

II. Whether the level of ordinary skill in the art has been properly ascertained under MPEP §2141.03.

7. Argument

I. Whether claims 1-29 are unpatentable under 35 U.S.C. §103(a) over Chevallier (U.S. Patent No. 5,898,634) in view of Mori et al. (U.S. Patent No. 6,891,214), and further in view of Perner (U.S. Patent No. 6,694,282).

To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP § 2143.01. Second, there must be a reasonable expectation of success. MPEP § 2143.02. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143.03. Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, none of the first, second, or third criteria described in MPEP § 2143 are satisfied. The combination of references does not teach or suggest all the claim limitations. Specifically, none of the references, alone and/or in combination, teach detecting input over-voltage conditions. Thus, none of the claims are obvious for at least this reason. Additionally, there is no motivation to combine the references since Chevallier describes a real-time adaptive feedback loop while Mori and Perner are unrelated to real-time feedback. Furthermore, it is unlikely that the proposed combination could be built due to overwhelming memory and space requirements and, if built, it likely could not provide the real-time adaptive feedback loop.

Mori

Mori describes storing over-current and over-temperature indications in a memory. (Mori et al., Column 7, Lines 4-53 and Column 10, Lines 30-35). The over-current condition

is obtained by monitoring the output current of a switching element. (Mori et al., Fig. 9 and Column 7, Lines 55-65). Mori is silent concerning acquiring and/or storing input operations conditions.

Perner

Perner describes storing calibration data (e.g., lower calibration temperature, upper calibration temperature) in a PROM during fabrication or as read form an external location at some other time. (Perner, Column 7, Lines 37-62 and Column 9, Lines 20-28). Perner is also silent concerning acquiring and/or storing input operation conditions (e.g., input voltage, Vcc).

Chevallier

Chevallier discloses an integrated circuit with a supply voltage detection circuit (Chevallier, Figure 2, DETECT 200) that produces an output that indicates a voltage range of the supply range. The output can be used in a feedback loop to adjust operation of the integrated circuit. (Chevallier, Abstract) The output may be a multiple bit code that identifies a supply voltage. The device also includes a status register latch for storing the multiple bit output signal. (Chevallier, Column 1, Lines 51-52). While Chevallier describes detecting a supply voltage, it simply reports this voltage, does not compare it to any "acceptable" value, and thus does not detect any out of specification condition. Consider Column 4, Lines 9-11, which reads "it may be desired to use a look up table for comparing output from the supply voltage detection circuit with recorded data to determine an operating voltage." This indicates that Chevallier is merely viewing the output signal from the detector in light of known reference values (e.g., 2.7V, 3.0V), to facilitate calibrating a voltage sensor to account for variations in a manufacturing process. However, this has nothing to do with detecting and/or recording an over-voltage condition because there is no comparison to any "good" or "good range" of values. The voltage is simply detected and temporarily stored in a latch register.

While the output signal can be compared to values in the lookup table, this is not used to detect an out of specification condition but rather as part of a feedback loop that will

"adjust the operation of the integrated circuit in response to the detected supply voltage range." (Chevallier, Column 5, Line 67 to Column 6, Line 8). The output can be stored in a latch, but the output is not data related to or describing an out of specification condition but rather is a simple description of the currently detected voltage without any out of specification property associated with or related to the value.

Therefore, Chevallier does not disclose detecting an over-voltage condition on any input and thus, it follows, also does not disclose recording any over-voltage condition. Chevallier simply detects and reports on a voltage range, completely disregarding whether the detected range is inside or outside a desired range.

The Office Action is incorrect when it asserts that the claims are obvious because "in reflect of the Vref of the IC is 2 volts, and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)." (Final Office Action, Page 2). This argument does not indicate that Chevallier discloses detecting an over voltage condition because the 2 volts given as an example is an example of an operating range for the integrated circuit for which calibration is data stored, not of an error (e.g., over voltage) condition. Furthermore, even if the 2 volts was outside a desired range, there is nothing in Chevallier that could detect that condition. For at least these reasons all the claims are not obvious over Chevallier, Mori, and Perner.

Claims will now be discussed individually.

Independent Claim 1

Claim 1 together with claims 2-11 were rejected in an omnibus rejection with the following rationale: "[t]he claimed method steps are interpreted and rejected as rejection stated above." (Final Office Action, Page 6). This rationale is somewhat difficult to understand leaving the Applicant with a less than meaningful opportunity to reply. Notwithstanding the deficiency in the rejection, the Chevallier/Mori/Perner combination does not teach each and every limitation found in independent claim 1. For example, none of the combinations, alone and/or in combination, teach storing data corresponding to an over-

voltage condition in an indelible memory as does claim 1. The only thing stored in Chevallier is an instantaneous voltage reading stored in a latch, which is completely unrelated to any error condition and which is discarded as soon as it is used in the adaptive real-time feedback loop. (Chevallier, Col. 5, Lines 63-65). Additionally, a person skilled in the art would not be motivated to store the voltage detected in Chevallier in a slow indelible memory because the voltage code is used as part of a substantially instantaneous feedback loop and is then discarded. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). The detected voltage in Chevallier is constantly being overwritten. Id. Burning a PROM or fuse would make the feedback loop in Chevallier too slow for practical use and would quickly consume inordinate amounts of memory with useless data. Imagine how many fuses would be burned in just one second of operation of the Chevallier/Mori/Perner combination. If the system operated at 100 MHz, then 100 million fuses would be burned or 100 million PROM locations would be forever altered in just one second. And all those fuses and PROM locations would store irrelevant information that would never be consulted because the combination would have moved on in its real-time adaptive feedback loop to look at the next voltage, not at any previous voltage.

Clearly the Chevallier/Mori/Perner combination is impractical at best, impossible to construct at worst, and worthless for any task if constructed. Thus, this claim is not obvious over the references and is in condition for allowance.

Independent claim 4

Claim 4 together with claims 1-11 were rejected in an omnibus rejection with the following rationale: "[t]he claimed method steps are interpreted and rejected as rejection stated above." (Final Office Action, Page 6). This rationale is somewhat difficult to understand leaving the Applicant with a less than meaningful opportunity to reply. Notwithstanding the deficiency in the rejection, the Chevallier/Mori/Perner combination does not teach each and every limitation found in independent claim 4. For example, none of the combinations, alone and/or in combination, teach comparing an input operational condition with a specified condition as does claim 4. The only thing stored in Chevallier is an

instantaneous voltage reading, which is completely unrelated to any error condition and which is discarded as soon as it is used in the adaptive real-time feedback loop. (Chevallier, Col. 5, Lines 63-65). Additionally, the arguments above concerning the fact that the combination of Chevallier/Mori/Perner likely could not be built and if built would be inoperative for its assigned task apply equally here. Thus, this claim is not obvious over the references and is in condition for allowance.

Dependent claim 7

Claim 7 was rejected in an omnibus rejection of claims 1-11 citing rejections to claims 12-29. (Final Office Action, Page 6). However, claim 7 includes elements or limitations not found in claims 12-29. Thus, this omnibus rejection actually provides no rejection at all for claim 7. Claim 7 includes the limitation that the specified amount of time is associated with a power on reset time. None of the references describe this limitation and none of the claims 12-29 describe this limitation. Thus, there is no rationale provided for rejecting claim 7.

Dependent claim 9

Claim 9 was rejected in an omnibus rejection of claims 1-11 citing rejections to claims 12-29. (Final Office Action, Page 6). However, claim 9 includes elements or limitations not found in claims 12-29. Thus, this omnibus rejection actually provides no rejection at all for claim 9. Claim 9 recites recording a clock speed. Not only do none of the references describe recording a clock speed, but none of claims 12-29 describe storing a clock speed. Thus, there is no rationale provided for rejecting claim 9.

Dependent claim 11

Claim 11 was rejected in an omnibus rejection of claims 1-11 citing rejections to claims 12-29. (Final Office Action, Page 6). However, claim 11 includes elements or

limitations not found in claims 12-29. Thus, this omnibus rejection actually provides no rejection at all for claim 11. Claim 11 recites reading a signature value stored in an indelible memory. None of the references describe this element and none of the claims 12-29 describe this element. Thus, there is no rationale given in the Office Action for rejecting claim 11.

Independent Claim 12

Claim 12 together with claims 17-18, and 21-22, were rejected using the same rationale, that in Chevallier "the detected variation input voltage range constitute of over-voltage conditions, in reflect of the Vref of the IC is 2 volts [see col. 1, lines 11-17, and col. 5, lines 40-67], and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)". (Final Office Action, Page 2). This quoted rationale is somewhat difficult to understand, which denies Applicant a meaningful opportunity to reply. What is clear, however, is that Chevallier is simply reporting on a detected voltage. The voltage described (e.g., Vref = 2 volts) is inside an operating range and used either for calibration or for a feedback loop, not for error detecting. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). A code for the detected voltage may be stored temporarily in a high-speed memory (e.g., register) to support the adaptive feedback loop. (Chevallier, Col. 5, Line 63 – Col. 6, Line 1). The code may be used to adapt an operating setting of the integrated circuit from which the voltage was detected. (Chevallier, Col. 6, Lines 1-10). But no error condition is detected or stored.

The Office Action uses Mori and Perner to establish that the voltage code could be stored in a permanent memory. (Final Office Action, Page 3). No-one skilled in the art would be motivated to store the voltage detected in Chevallier in a slow permanent memory because the voltage code is used as part of a substantially instantaneous feedback loop and is then discarded. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). The detected voltage is constantly being overwritten. Burning a PROM or fuse would make the feedback loop in Chevallier too slow for practical use and would quickly consume inordinate amounts of memory with useless data. Imagine how many fuses would be burned in just one second of operation of the Chevallier/Mori/Perner combination. If the system operated at 100 MHz,

then 100 million fuses would be burned or 100 million PROM locations would be forever altered in just one second. And all those fuses and PROM locations would store irrelevant information that would never be consulted because the combination would have moved on in its real-time adaptive feedback loop to look at the next voltage, not at any previous voltage.

Clearly the Chevallier/Mori/Perner combination is impractical at best, impossible to construct at worst, and worthless for any task if constructed. For at least these reasons the claims are not obvious and are in condition for allowance.

Dependent claim 13

Claim 13 recites filtering an input operational voltage for at least a duration of one clock period, which the Office Action asserts would have been obvious to add. (Final Office Action, Pages 3-4). The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this reason, this claim is not obvious and is in condition for allowance.

Dependent claim 14

This claim recites only recording the over-voltage condition if the operational voltage exceeds the specified voltage by a selected amount, which the Office Action asserts would have been obvious to add. (Final Office Action, Page 4). The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this reason, this claim is not obvious and is in condition for allowance.

Dependent claim 15

This claim recites only recording the over-voltage condition if the operational voltage exceeds the specified voltage by at least two times an expected noise voltage value, which the Office Action asserts would have been obvious to add. (Final Office Action, Page 4). The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. Additionally, the rationale provided concerns the limitation in claim 14, not the additional limitation in claim 15. For at least these reasons this claim is not obvious and is in condition for allowance.

Dependent claim 16

This claim recites verifying recordation of the input operating over-voltage condition, which the Office Action asserts would have been obvious to add. (Final Office Action, Page 4). The Office Action provides a rationale for this official notice but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. No motivation could possibly be found for verifying the recordation in the Chevallier/Mori/Perner combination since the combination describes a real-time adaptive feedback loop. Verifying the recordation would likely slow down the feedback loop so much that the instantaneous adaptation would be lost, rendering the machine worthless for its appointed task. For at least this reason this claim is not obvious and is in condition for allowance.

Independent claim 17

Claim 17 was rejected together with claims 12, 18, and 21-22, using the same rationale, that in Chevallier "the detected variation input voltage range constitute of over-

voltage conditions, in reflect of the Vref of the IC is 2 volts [see col. 1, lines 11-17, and col. 5, lines 40-67], and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)." (Final Office Action, Page 2).

This quoted rationale is somewhat difficult to understand, which denies Applicant a meaningful opportunity to reply. What is clear, however, is that the cited text of Chevallier is simply reporting on a detected voltage. The voltage described (e.g., Vref = 2 volts) is inside an operating range and used either for calibration or for a feedback loop, not for error detecting. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). A code for the detected voltage may be stored temporarily in a high-speed memory (e.g., register) to support the adaptive feedback loop. (Chevallier, Col. 5, Line 63 – Col. 6, Line 1). The code may be used to adapt an operating setting of the integrated circuit from which the voltage was detected. (Chevallier, Col. 6, Lines 1-10). But no error condition is detected or stored.

The Office Action uses Mori and Perner to establish that the voltage code could be stored in a permanent memory. No-one skilled in the art would be motivated to store the voltage detected in Chevallier in a slow permanent memory because the voltage code is used as part of a substantially instantaneous feedback loop and is then discarded. The detected voltage is constantly being overwritten. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). Burning a PROM or fuse would make the feedback loop in Chevallier too slow for practical use and would quickly consume inordinate amounts of memory with useless data. Imagine how many fuses would be burned in just one second of operation of the Chevallier/Mori/Perner combination. If the system operated at 100 MHz, then 100 million fuses would be burned or 100 million PROM locations would be forever altered in just one second. And all those fuses and PROM locations would store irrelevant information that would never be consulted because the combination would have moved on in its real-time adaptive feedback loop to look at the next voltage, not at any previous voltage.

Clearly the Chevallier/Mori/Perner combination is impractical at best, impossible to construct at worst, and worthless for any task if constructed. For at least these reasons the claims are not obvious and are in condition for allowance.

Dependent claim 19

This claim recites a filter module, which the Final Office Action asserts would have been obvious to add. (Final Office Action, Pages 3-4). The Office Action provides a rationale for this official notice, but provides no citation to any of the three references that provides any motivation. A teaching, suggestion, or motivation must be found somewhere and cannot be created after the fact using hindsight reconstruction. For at least this reason this claim is not obvious and is in condition for allowance.

Independent Claim 22

Claim 22 together with claims 12, 17-18, and 21 were rejected using the same rationale, that in Chevallier "the detected variation input voltage range constitute of over-voltage conditions, in reflect of the Vref of the IC is 2 volts [see col. 1, lines 11-17, and col. 5, lines 40-67], and the detected over-voltage conditions output being recorded in the memory met by a (status register latch)". (Final Office Action, Page 2).

This quoted rationale is somewhat difficult to understand, which denies Applicant a meaningful opportunity to reply. What is clear, however, is that Chevallier is simply reporting on a detected voltage. The voltage described (e.g., Vref = 2 volts) is inside an operating range and used either for calibration or for a feedback loop, not for error detecting. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23). A code for the detected voltage may be stored temporarily in a high-speed memory (e.g., register) to support the adaptive feedback loop. (Chevallier, Col. 5, Line 63 – Col. 6, Line 1). The code may be used to adapt an operating setting of the integrated circuit from which the voltage was detected. (Chevallier, Col. 6, Lines 1-10). But no error condition is detected or stored.

The Office Action uses Mori and Perner to establish that the voltage code could be stored in a permanent memory. No-one skilled in the art would be motivated to store the voltage detected in Chevallier in a slow permanent memory because the voltage code is used as part of a substantially instantaneous feedback loop and is then discarded. The detected voltage is constantly being overwritten. (Chevallier, Col. 3, Line 28 – Col. 6, Line 23).

Burning a PROM or fuse would make the feedback loop in Chevallier too slow for practical use and would quickly consume inordinate amounts of memory with useless data. Imagine how many fuses would be burned in just one second of operation of the Chevallier/Mori/Perner combination. If the system operated at 100 MHz, then 100 million fuses would be burned or 100 million PROM locations would be forever altered in just one second. And all those fuses and PROM locations would store irrelevant information that would never be consulted because the combination would have moved on in its real-time adaptive feedback loop to look at the next voltage, not at any previous voltage.

Clearly the Chevallier/Mori/Perner combination is impractical at best, impossible to construct at worst, and worthless for any task if constructed. For at least these reasons the claims are not obvious and are in condition for allowance.

Dependent claim 29

This claim recites that the system includes a BIOS to determine the selected number of out-of-specification input operational conditions to detect. The Office Action simply asserts that Mori discloses a BIOS. (Final Office Action, Page 6). Simply have a BIOS does not mean that the BIOS is configured to determine the number of out-of-specification conditions to detect. Neither Mori nor any of the other references teach this element. For at least this reason this claim is not obvious and is condition for allowance.

II. Whether the level of ordinary skill in the art has been properly ascertained under MPEP §2141.03.

MPEP §2141.03 requires that the Office Action ascertain and describe the level of ordinary skill so that objectivity can be maintained. MPEP §2141.03 reads:

> The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry. *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718, 21 USPQ2d 1053, 1057 (Fed. Cir. 1991). The examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made, and not to the inventor, a judge, a layman, those skilled in remote arts, or to geniuses in the art at hand. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), cert. denied, 464 U.S. 1043 (1984).

Here the Office Action neither ascertains nor reports on the level of ordinary skill in the art. The skill level has not been ascertained. For this additional reason, the rejections are improper and should be withdrawn.

Conclusion

For the reasons set forth above, a prima facie obviousness rejection has not been established for any claim. All rejections have been shown to be improper. Appellant respectfully believes that all pending claims **1-29** patentably and unobviously distinguish over the references of record and that the rejections should be withdrawn. Appellant respectfully requests that the Board of Appeals overturn the Examiner's rejections and allow all pending claims. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

10-31-07

Date

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8. Claims Appendix

1. A method, comprising:

storing data corresponding to at least one input operating over-voltage condition occurring in an integrated circuit in an indelible memory.

2. The method of claim 1, further comprising:

determining a specified number of stored over-voltage conditions.

3. The method of claim 2, further comprising:

indicating the specified number of stored over-voltage conditions.

4. A method, comprising:

comparing an input operational condition with a specified condition:

recording data corresponding to an out-of-specification input operating condition in an indelible memory; and

determining a specified number of recorded out-of-specification input operating conditions.

5. The method of claim 4, further comprising:

detecting the out-of-specification input operating condition as an input operating over-voltage condition.

6. The method of claim 4, further comprising:

refraining from detecting the out-of-specification input operating condition for a specified amount of time.

7. The method of claim 6, wherein the specified amount of time is associated with a power-on reset time.

8. The method of claim 4, wherein the specified condition comprises a recommended operational input voltage upper limit associated with an integrated circuit.

9. The method of claim 4, wherein recording the out-of-specification input operating condition further comprises:

recording a clock speed.

10. The method of claim 9, wherein the indelible memory comprises at least one fuse.

11. The method of claim 4, wherein determining the specified number of recorded out-of-specification input operating conditions further comprises:

reading a signature value stored in the indelible memory.

12. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

comparing an input operational voltage with a specified voltage;

recording a value corresponding to an input operating over-voltage condition in an indelible memory; and

determining a specified number of recorded input operating over-voltage conditions.

13. The article of claim 12, wherein the data, when accessed, results in the machine performing:

filtering the input operational voltage for at least a duration of one clock period.

14. The article of claim 12, wherein recording the value corresponding to the input operating over-voltage condition further comprises:

recording the value corresponding to the input operating over-voltage condition only if the input operational voltage is greater than the specified voltage by a selected amount.

15. The article of claim 14, wherein the selected amount is at least about two times greater than an expected noise voltage value.

16. The article of claim 12, wherein the data, when accessed, results in the machine performing:

verifying recordation of the value corresponding to the input operating over-voltage condition.

17. An apparatus, comprising:

an indelible memory to store information corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit.

18. The apparatus of claim 17, further comprising:

a detection module coupled to the indelible memory to determine the existence of at least one of the selected number of out-of-specification input operational conditions.

19. The apparatus of claim 18, further comprising:

a filter module coupled to the detection module.

20. The apparatus of claim 17, wherein the indelible memory comprises a fuse.

21. The apparatus of claim 17, wherein at least one of the out-of-specification input operational conditions comprises an over-voltage condition.

22. A system, comprising:

an indelible memory to store data corresponding to a selected number of out-of-specification input operational conditions encountered by an electronic circuit; and

a display coupled to the electronic circuit.

23. The system of claim 22, wherein the electronic circuit comprises a microprocessor.

24. The system of claim 22, further comprising:

a logic module to detect each one of the selected number of out-of-specification input operational conditions.

25. The system of claim 24, wherein the logic module comprises an analog-to-digital converter.

26. The system of claim 22, further comprising:

a second memory to store data corresponding to a specified condition to be compared with an operational condition associated with the electronic circuit.

27. The system of claim 26, wherein the specified condition comprises a recommended operational input voltage upper limit associated with an integrated circuit.

28. The system of claim 27, wherein the integrated circuit comprises a microprocessor.

29. The system of claim 22, further comprising:

a basic input-output system to determine the selected number of out-of-specification input operational conditions.

9. Evidence Appendix

None. There is no extrinsic evidence.

10. Related Proceedings Appendix

None. There are no related proceedings.